Remarks

Claims 1-14, 24-31, 33-38, 47-50, 52, 112-119, 124-127, 137-139, 141, 144, 146, and 149-161 are pending.

Claims 1-4, 6, 24-25, 29, 33-35, 48, 112, 124, 149-152, and 156-159 have been amended to clarify the subject matter claimed.

New Claims 162-164 have been added.

No new matter has been added with the amendments to the claims or the addition of the new claims. The amendments are intended to merely clarify language used in the claims and the subject matter claimed, and the scope of the claims is intended to be the same as before the amendment.

Rejection under 35 U.S.C. § 102(b) (Tuckerman) (Akram)

The Examiner rejected Claims 1-7, 11, 24-25, 33, 112-114, 124, 125, 144, 146, 149-153, and 160 under Section 102(b) as anticipated by Tuckerman, USP 5,804,004. The Examiner also rejected Claims 1-4, 24-25, 33, 112, 124, 144, 146, 149-153, and 160 as anticipated by Akram, USP 6,351,028. These rejections are respectfully traversed.

Tuckerman, USP 5,804,004. The Examiner cites particularly to FIGS. 4A and 8 of Tuckerman as disclosing all of the elements of the claims.

Tuckerman teaches dies having a bottom surface with a beveled edge to provide clearance for a wire lead of the lower chip, as depicted in **FIGS. 4A and 8** below.

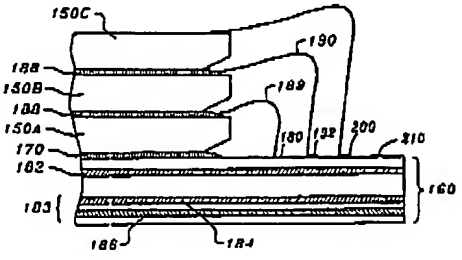


FIG. 4A.

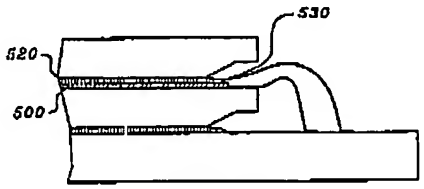
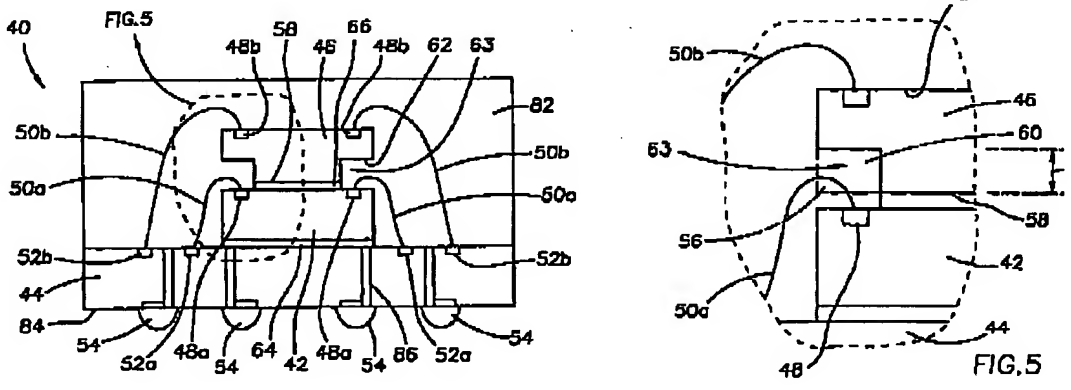


FIG. 8.

Although Tuckerman states that the integrated circuit includes a "recessed bottom surface," Tuckerman specifically teaches a beveled edge and low profile wire bonding such that the wires are nearly parallel to the chip surface to keep a *low loop profile* and a relatively *flat* horizontal component (at col. 3, lines 2-21, and col. 5, lines 5-11 and 19-20 (emphasis added)). Tuckerman further teaches that the bevel angle is preferably *a 35° angle* (at cols. 3-4, bridging paragraph (emphasis added)).

> As seen in FIG. 4A, ...A wire bonding process employing reverse wedge bonding is preferred, as it provides low loop height and a shallow exit angle of the wires in the vicinity of the chip bond pad. The wires are nearly parallel to the chip surface. ...
>
> In the embodiment shown in FIG. 4A, wire leads 189 and 190 are prevented from making contact with the adjacent upper chip by beveling the edge of the upper chip. The bevel extends from the chip edge inward to a distance beyond the chip bond pad of the chip below. In a preferred embodiment, *the bevel angle is approximately 35°. The 35° angle* typically exceeds the exit angle of the adjacent wire lead and ensures proper clearance.
>
> In step 420, IC 150a is then wire bonded to bond pads located on the silicon circuit board 160. ...The loop profile is kept low and has a steep vertical ascent and relatively flat horizontal component. The low profile minimizes the amount of beveling required on the upper chips to preclude contact between the wires and the silicon. When the chip is approximately 10-20 mils thick, a chip to bond pad clearance of 20-25 mils proves acceptable.
>
> After the die attach adhesive is cured, *low profile wire bonding* of the chip 150b is performed in step 440.

By comparison, in Applicant's die assembly as claimed, the upper (second) die has a *non*-beveled edge along the perimeter. This is illustrated, for example, in **FIGS. 4-5** below — showing a non-beveled edge (**62**) and an opening (**63**) along the perimeter (**56**) of the upper (second) die (**46**).



Tuckerman does not teach or suggest a die assembly as claimed by Applicant. Accordingly, withdrawal of this rejection is respectfully requested.

Akram, USP 6,351,028. The Examiner also cites to Akram as disclosing all of the elements of the claims.

Akram discloses a die stack that incorporates T-shaped interposer elements.

In Akram's assembly, *dies* **24** are stacked on *T-shaped spacers or interposers* **26**, as shown below in **FIGS. 2 and 4**, and described at col. 2, lines 53-58, and col. 3, lines 27-34 (emphasis added).

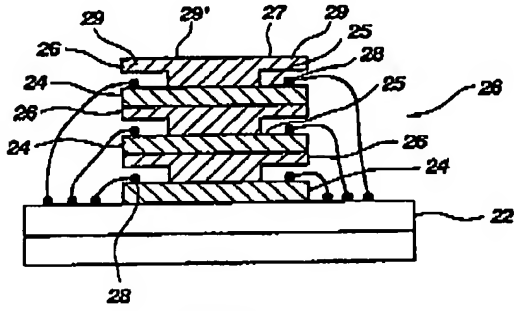


Fig. 2

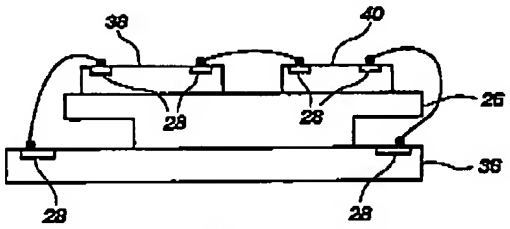


Fig. 4

SUMMARY OF THE INVENTION

...The present invention relates to multiple integrated circuit devices in a stacked configuration that *uses a spacing element* for allowing increased device density and the removal of thermal energy from semiconductor devices and the methods for the stacking thereof.

...

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENT

Illustrated in a cross-sectional diagram in drawing **FIG. 2** is a multi-stacked semiconductor device structure utilizing *a T-interposer device* having a T-shape in cross-section of the present invention. Multiple stack unit 20 comprises a substrate 22, a first semiconductor device 24 disposed on substrate 22, a first T-interposer 26 disposed on the first semiconductor device 24, *and multiple semiconductor devices 24 disposed on multiple T-interposers 26*. Each semiconductor device 24 includes a plurality of bond pads 28 thereon. ...Each semiconductor device 24 is subsequently stacked one on top of another in a horizontal plane *with a T-interposer 26 disposed between each semiconductor device 24*.

Akram teaches an assembly having T-shaped *spacers* between dies. That disclosure does not teach or suggest a die assembly as claimed by Applicant in which a *die* having a non-beveled recessed edge along a perimeter is stacked on another die.

Accordingly, withdrawal of this rejection is respectfully requested.

Rejection under 35 U.S.C. § 103(a) (Tuckerman, Zuhr)

The Examiner rejected Claims 8, 9, 26-27, 30-31, 37-38, 52, 119, 126-127, 137-139, 141, 144, and 153 as obvious over Tuckerman in view of Zuhr (DE 10209204). This rejection is respectfully traversed.

The present application USSN 10/068,159, was filed **February 5, 2002.**

Zuhr has been improperly cited against this application. Zuhr was published on **October 2, 2003,** *after* both the priority date and the filing date of the present application.

Accordingly, withdrawal of this rejection is respectfully requested.

Extension of Term. The proceedings herein are for a patent application and the provisions of 37 CFR § 1.136 apply. Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that Applicant has inadvertently overlooked the need for a petition for extension of time. If any extension and/or fee are required, please charge Account No. 23-2053.

It is respectfully submitted that the claims are in condition for allowance and notification to that effect is earnestly solicited. The Examiner is urged to telephone the undersigned attorney if any questions should arise.

Respectfully submitted,

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Dated: November 16, 2005

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